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Colleen J. Dew

13 | Appeal Brief 7-16-03 A. Walker

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2822

In re application of	:	June 30, 2003
Axel Brintzinger et al.	:	Examiner: Monica Lewis
Serial No.: 09/873,537	:	
Filed: June 4, 2001	:	IBM Corporation Dept. 18G/Bldg, 300-482
Title: DUAL DAMASCENE ANTI-FUSE WITH VIA BEFORE WIRE	:	2070 Route 52 Hopewell Junction, NY 12533-6531

APPEAL BRIEF

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TECHNOLOGY CENTER 2800

Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

This is an appeal from the Final Rejection of claims 22-30. A correct copy of the claims is attached in the Appendix.

Real Party in Interest

The real parties in interest are International Business Machines Corporation per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 011199/0187 on October 16, 2000 and Infineon Technologies North America Corp. per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 011198/0060 on October 16, 2000.

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Related Appeals and Interferences

None.

Status of Claims

Claims 22-30 are pending.

Status of Amendments

No amendments after Final Rejection have been submitted.

Summary of Invention

The invention centers on novel interconnect structures having an anti-fuse formed as a layer having openings that define via locations. The structures of the invention advantageously incorporate anti-fuses at reduced manufacturing cost. See the specification at page 4, lines 10-29, Figures 2e, 2f and 3, .

Issues

1. Whether claims 22-24, 26, 27, 29 and 30 are patentable under 35 USC 103(a) over Boardman et al. (US Pat. 5120679) in view of Chang (US Pat. 5565703).

2. Whether claim 25 is patentable under 35 USC 103(a) over Boardman et al. (US Pat. 5120679) in view of Chang (US Pat. 5565703) and Go et al. (US Pat. 5592016).

3. Whether claim 28 is patentable under 35 USC 103(a) over Boardman et al. (US Pat. 5120679) in view of Chang (US Pat. 5565703) and McCollum et al. (US Pat. 5770885).

Grouping of Claims

The claims stand or fall together within each respective issue identified above.

Argument

1. Whether claims 22-24, 26, 27, 29 and 30 are patentable under 35 USC 103(a) over Boardman et al. (US Pat. 5120679) in view of Chang (US Pat. 5565703).

Boardman et al. (US 5120679) discloses a structure where the vias are defined by holes in thick dielectric layer 46. The antifuse layer 52 is removed from all locations except for holes where the antifuses are desired. See Figures 3c-3f. Boardman et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Chang (US 5565703) discloses an antifuse structure where a dielectric layer 37) is deposited over the periphery of an antifuse layer 36 to define a location of a conductive plug 50. Chang does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

It is not apparent why one would seek to put an additional dielectric layer over the antifuse layer of Boardman et al. as proposed in the official action. There is no apparent utility that would be achieved. If anything, such a combination would render the antifuse of Boardman et al. inoperative. Appellants submit that the combination of these references would at best result in replacement of the Boardman et al. antifuse structure with that of Chang. In no case would such a combination result in the claimed invention where an anti-fuse layer with an opening which defines a via location.

2. Whether claim 25 is patentable under 35 USC 103(a) over Boardman et al. (US Pat. 5120679) in view of Chang (US Pat. 5565703) and Go et al. (US Pat. 5592016).

Boardman et al. (US 5120679) discloses a structure where the vias are defined by holes in thick dielectric layer 46. The antifuse layer 52 is removed from all locations except for holes where the antifuses are desired. See Figures 3c-3f. Boardman et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Chang (US 5565703) discloses an antifuse structure where a dielectric layer 37) is deposited over the periphery of an antifuse layer 36 to define a location of a conductive plug 50. Chang does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Go et al. (US 5592016) discloses anti-fuse structures which are located above or below vias. Go et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

It is not apparent why one would seek to put an additional dielectric layer over the antifuse layer of Boardman et al. in view of Chang as proposed in the official action. There is no apparent utility that would be achieved. If anything, such a combination would render the antifuse of Boardman et al. inoperative. Appellants submit that the combination of these references (Boardman et al., Chang, and Go et al.) would at best result in replacement of the Boardman et al. antifuse structure with that of Chang with the use of the polyimide dielectrics of Go et al. In no case would such a combination result in the claimed invention where an anti-fuse layer with an opening which defines a via location.

3. Whether claim 28 is patentable under 35 USC 103(a) over Boardman et al. (US Pat. 5120679) in view of Chang (US Pat. 5565703) and McCollum et al. (US Pat. 5770885).

Boardman et al. (US 5120679) discloses a structure where the vias are defined by holes in thick dielectric layer 46. The antifuse layer 52 is removed from all locations except for holes where the antifuses are desired. See Figures 3c-3f. Boardman et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Chang (US 5565703) discloses an antifuse structure where a dielectric layer 37) is deposited over the periphery of an antifuse layer 36 to define a location of a conductive plug 50. Chang does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

McCollum et al. (US 5770885) discloses a silicon oxynitride layer on a substrate over which an amorphous silicon anti-fuse is formed. McCollum et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

It is not apparent why one would seek to put an additional dielectric layer over the antifuse layer of Boardman et al. in view of Chang as proposed in the official action. There is no apparent utility that would be achieved. If anything, such a combination would render the antifuse of Boardman et al. inoperative. Appellants submit that the combination of these references (Boardman et al., Chang, and McCollum et al.) would at best result in replacement of the Boardman et al. antifuse structure with that of Chang with the use of the oxynitride of McCollum et al. as part of the antifuse stack. In no case would such a combination result in the claimed invention where an anti-fuse layer with an opening which defines a via location.

Conclusion

Based on the above arguments, appellants submit that the present claims are patentable over the prior art of record that the rejections under 35 USC 103(a) should be reversed.

Respectfully submitted,
Axel Brintzinger et al.

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Appendix

Claims on Appeal

22. An interconnect structure in which an anti-fuse dielectric is formed therein comprising:

a substrate having a first level of electrically conductive features;

a patterned anti-fuse dielectric layer formed on said substrate, wherein said patterned anti-fuse dielectric layer includes an opening to at least one of said first level of electrically conductive features;

a patterned interlevel dielectric material formed on said patterned anti-fuse dielectric layer, wherein said patterned interlevel dielectric

includes vias, at least one of said vias has a via space formed above said opening; and

a second level of electrically conductive features formed in said vias and via space(s).

23. The interconnect structure of Claim 22 wherein said substrate is composed of an interlevel dielectric material that is the same or different from said patterned interlevel dielectric material.

24. The interconnect structure of Claim 22 wherein said patterned interlevel dielectric material is composed of an inorganic semiconductor material selected from the group consisting of SiO_2, Si_3N_4, diamond, diamond-like carbon and fluorinated doped oxides.

25. The interconnect structure of Claim 22 wherein said patterned interlevel dielectric material is composed of an organic dielectric material selected from the group consisting of polyimides, polyamides, paralyene and polymethylmethacrylate.

26. The interconnect structure of Claim 22 wherein said first and second levels of electrically conductive features are composed of the same or different conductive metal selected from the group consisting of aluminum, tungsten, copper, chromium, gold, platinum, palladium and alloys, mixtures and complexes thereof.

27. The interconnect structure of Claim 22 wherein said anti-fuse dielectric layer is a dielectric material selected from the group consisting of SiO_2, Si_3N_4, Si oxynitrides, amorphous Si, amorphous C, H-containing dielectrics, carbon, germanium, selenium, compound semiconductors, ceramics and anti-reflective coatings.

28. The interconnect structure of Claim 27 wherein said anti-reflective coating is silicon oxynitride.

29. The interconnect structure of Claim 22 wherein another interconnect level is formed over said patterned interlevel dielectric layer.

30. The interconnect structure of Claim 29 wherein said another interconnect level includes a tapered metal contact region.

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